AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows. Insertions appear as underlined text (e.g., insertions) while deletions appear as strikethrough text (e.g., ~~deletions~~).

Please replace Page 13 second paragraph with the following rewritten paragraph:

> Figure 1 is a block diagram showing a multi-channel medium 112 connecting a multi-channel transmitter 111 to a multi-channel receiver 113. The multi-channel medium 112 is configured to provide *m* separate data channels 101-103 shown as a first channel 101, a second channel 102, and an ***M*-th** ~~m-th~~ channel 103. The multi-channel transmitter 111 provides a separate data output to each channel 101-103 and each of the multi-channels 101-103 is provided to a separate data input of the multi-channel receiver 113. In one embodiment, the multi-channel transmitter 111 receives a single logical input data stream and separates the input data stream into *M* data streams, one stream for each of the *M* channels. Similarly, the multi-channel receiver 113 receives the data from the multi-channel transmitter 111 on *M* data streams and combines the received data into a single logical output stream. In one embodiment, the multi-channel transmitter 111 receives multiple data streams and the receiver 113 outputs multiple data streams. The multi-channel medium 112 can be, for example, a wire, a cable, an optical fiber, a coaxial cable, a waveguide, a radio-frequency propagation path, an optical propagation path, a twisted pair cable, etc.

Please replace Page 14 first paragraph with the following rewritten paragraph:

> Figure 2 shows a frequency spectrum of a conventional FDM system having a first channel corresponding to a carrier frequency f_i and a second channel corresponding to a carrier frequency f_{i+1}. The modulated spectrum of the first channel (being the spectrum obtained by modulation of the carrier $\underline{f_i}$ ~~f_i~~), includes a first channel main lobe 201, first upper and lower sidelobes 211 and 212

respectively, and second upper and lower sidelobes 213 and 214 respectively. The modulated spectrum of the second channel (being the spectrum obtained by modulation of the carrier f_{i+1}), includes a second channel main lobe 202, first upper and lower sidelobes 221 and 222 respectively, and second upper and lower sidelobes 223 and 224 respectively.

Please replace Page 15 third paragraph with the following rewritten paragraph:

Figure 3B shows a Fourier Transform based OFDM system that includes a transmitter 311 and a receiver 313. The transmitter 311 includes a modulator 320, an IFFT 321, a parallel-to-serial converter 331 and a D/A (Digital to Analog converter) 322. The receiver 312 includes an A/D (Analog to Digital converter) 323, a serial-to-parallel converter 332, an FFT 324, a demodulator 325. Input data is provided to an input of the modulator 320. The modulator 320 assigns data bits (symbols) to each of the carriers, and modulates the carriers accordingly. The carriers are provided to the IFFT 321. The IFFT 321 converts the carriers (frequency domain) into samples (time domain). The time domain samples are serialized by the parallel-to-serial converter 331 and provided to the D/A 322. The analog output of the D/A is provided, via the medium 112, to the A/D 323. The A/D 323 converts the analog samples into digital samples. The digital samples are converted from serial to parallel streams by the serial-to-parallel converter **332** ~~323~~ and provided to the FFT 324. The FFT 324 converts the digital samples (time domain) back into modulated carriers. The modulated carriers are provided to the demodulator 325. The demodulator 325 demodulates the carriers to extract the output data. One skilled in the art will recognize that other conventional operations, such as framing, blocking, and error correction can also be provided.

Please replace Page 18 fourth paragraph with the following rewritten paragraph:

The block processing nature of the IFFT 321 and the FFT **324** ~~323~~ means that the multipath effects of all channels must die out before the next symbol can be

transmitted on any channel. Thus, as shown in Figure 6, the guard time N_g must be extended to include the group delay effects of the channel showing the longest group delay. This is also illustrated in Figure 7, where it is shown that the IFFT 321 and the FFT **324** ~~323~~ within a time-frequency block 701. A frequency axis of the block 701 corresponds to the *M* frequency bins corresponding to the *M* channels. A time axis of the block 701 corresponds to the N_s samples of a symbol time. Of the N_s samples, N_b samples are used in the FFT block 324 (where N_b = *M*).

Please replace Page 19 first paragraph with the following rewritten paragraph:

By operating in the block 701, the FFT **324** ~~323~~ assures global orthogonality among all of the sub-carriers 0 through *M-1*. Thus for example, the FFT **324** ~~323~~ assures that the first channel with sub-carrier operating a at a frequency f_0 is orthogonal to (i.e. does not interfere with) the (*M-1*)th channel with sub-carrier operating at a frequency f_{M-1}. The penalty for global orthogonality is that the guard period must be long enough to deal with the variation in delay spreads among all channels and is therefore dictated by the maximum delay spread. Fortunately, global orthogonality is not necessary. As shown in Figure 2, the sidelobes of a carrier are attenuated at frequencies removed from the carrier frequency. Thus, in many circumstances, the sub-carrier operating at frequency f_0 and the sub-carrier operating at frequency f_{M-1} do not need to be orthogonal, because the main sidelobes of the carrier f_0 do not interfere with the main lobe of the carrier f_{M-1} and vice versa. In many circumstances, only adjacent carriers, or nearby carriers need to be orthogonal to avoid any noticeable inter-channel interference.

Please replace Page 22 second paragraph with the following rewritten paragraph:

Figure 9B shows the sliding-window transform system of Figure 9A extended to multiple channels. In Figure 9B the output of the A/D 323 is provided to an input of a *M*-th sliding-window transform 921, a second sliding-window transform 923,

and an *M*-th sliding window transform **923** ~~922~~. An output of the first sliding-window transform 921 is provided to an input of a first demapper 931. An output of the second sliding-window transform 921 is provided to an input of a second demapper 932. An output of the **M**-th ~~first~~ sliding-window transform 921 is provided to an input of an *M*-th demapper 933.

Please replace Page 22 third paragraph with the following rewritten paragraph:

Figure 10A is a block diagram of a sliding-window receiver 1000 that uses a Type-1 DFT transform. The receiver 1000 is one embodiment of the receiver 913 shown in Figure 9**A**. The communication channel 112 is provided to an input of a coupler 1050. An output of the coupler 1050 is provided to an input of an optional sub-band filter 1051. An output of the filter 1051 is provided to an analog input of the analog-to-digital converter 323. In receiver 1000, the DFT 924 includes an adjustable N-word shift register 1010 having an adjustable tap 1016 that determines N. The shift register 1010 stores N n-bit words provided by the A/D 323. Each new digital sample from the A/D 323 is provided to a first word in the register 1010 and to a non-inverting input of an adder 1011. As each new sample is received, shift register 1010 shifts right one word. A last word of the shift register 1010 is provided to an inverting input of the adder 1011. An output of the adder 1011 is provided to a first input of an adder 1012 and to a first input of an adder 1022.

Please replace Page 23 first paragraph with the following rewritten paragraph:

An output of the adder 1012 is provided to a first input of a multiplier 1013. A complex constant φ_0 is provided to a second input of the multiplier 1013. The constant multiplier is calculated according to the equation

$$\phi_i = e^{\frac{-j2\pi k_i}{N}} \qquad \overline{\phi_i = e^{\frac{j2\pi k_i}{N}}}$$

where i is the channel, ~~k_i~~ k_i is the wave number for the carrier frequency represented by the channel i, and N is the number of samples.

Please replace Page 23 fourth paragraph with the following rewritten paragraph:

Figure 10B is a block diagram of a sliding-window receiver 1080 that uses a Type-2 Fourier transform. The receiver 1080 is one embodiment of the receiver 913 shown in Figure 9A. The receiver 1080 is similar to the receiver 1000, except in the ordering of the adders 1012, 1022 and the multipliers 1013,1023. In the receiver 1080, the output of the adder 1011 is provided to the first input of the multipliers 1013 and 1023. The complex sinusoid $e^{\frac{-j2\pi k_0 n}{N}}$ $e^{\frac{-j2\pi k_i n}{N}}$ is provided to a second input of the multiplier 1013. The output of the multiplier 1013 is provided to the first input of the adder 1012. The complex constant φ_{M-1} is provided to a second input of the multiplier 1023. The output of the multiplier 1023 is provided to the first input of the adder 1022.

Please replace Page 25 second paragraph with the following rewritten paragraph:

Figure 11 shows an alternate embodiment of the adjustable shift register 1010. As shown in Figure 11, the value of N (the number of words used in the DFT operation) can be easily varied by changing the output tap on the shift register 1010. In Figure 11, the input to the inverting input of the adder 1011 is taken from a selected tap on of the shift register 1010 rather than the last tap. The value N (the length of the basis function) is the number of taps between the input tap and the output tap. The value of N can be reduced for shorter symbol times (corresponding to higher symbol rates) and the value of N can be lengthened for longer symbol times (corresponding to slower symbol rates). The adder 1011 can be replicated across all of the M channels to provide selection of the basis function length N independently on each channel. The basis function coefficients ϕ_i shown in Figure 10A, and in the above equation also depend on N. Thus, when N is

changed for a specific channel, ϕ_i should typically be changed for that channel as well.

Please replace Page 26 first paragraph with the following rewritten paragraph:

The packet-header detector 1202 receives signals from the demodulator via the multiplier **1201** ~~1202~~. The equalization calculator initially sets the equalization coefficient to a known value, such as, for example unity. The packet-header detector 1202 detects a packet preamble by searching for a predefined bit pattern in the received signals from the demodulator 1030. When the packet-header detector 1202 detects the bit pattern as a preamble vector $\boldsymbol{p}_r$ having an amplitude and a phase. In one embodiment, the packet-header detector 1202 detects the preamble using a correlation process that outputs a correlation value as the preamble vector $\boldsymbol{p}_r$. In one embodiment, the packet-header detector 1202 detects the preamble using a preamble filter that outputs a filter value as the preamble vector $\boldsymbol{p}_r$. In one embodiment, the preamble filter is an adaptive filter. The received preamble vector $\boldsymbol{p}_r$ is provided to the equalization calculator 1206, and a start-of-packet command is sent to the symbol detector 1203.

Please replace Page 27 second paragraph with the following rewritten paragraph:

The packet-header detector 1202 receives signals from the demodulator via the multiplier **1201** ~~1202~~. As in the equalizer system shown in Figure 12, in Figure 13 the equalization calculator 1306 initially sets the equalization coefficient to a known value, such as, for example unity. The packet-header detector 1202 detects a packet preamble by searching for a predefined bit pattern in the received signals from the demodulator 1030. When the packet-header detector 1202 detects the bit pattern as a preamble vector v_r having an amplitude and phase. The received preamble vector $\boldsymbol{p}_r$ is provided to the equalization calculator 1306, and a start-of-packet command is sent to the symbol detector **1303** ~~1203~~.

Please replace Page 28 first paragraph with the following rewritten paragraph:

After receiving the start-packet command from the packet-header detector 1202, the symbol detector **1303** ~~1203~~ received equalized data, extracts the first symbol from the equalized data, and provides the symbol to the packet framer 1204. The symbol detector **1303** ~~1203~~ also provides a received symbol vector s_r and an expected symbol vector s_e as symbol equalization data to the equalization calculator 1306. The received symbol vector s_r is the actual vector detected for the received symbol, and the vector s_e is the expected vector for that symbol. Upon receiving the vectors s_r and s_e the equalization calculator 1306 recalculates the equalization coefficient and provides the equalization coefficient to the multiplier 1201 to equalize the data for the next symbol.

Please replace Page 32 first paragraph with the following rewritten paragraph:

Figure 14 is a block diagram of a multi-band transmitter 1400 for use with a multi-band sliding-window receiver. In the transmitter 1400, data for a first channel (i.e., channel 0) of an M-channel band (i.e., Band 0) is provided to an input of an FEC block 1402. An output of the FEC block 1402 is provided to an input of an interleaver/scrambler block 1403. An output of the block 1403 is provided to an input of a modulator/mapper block 1404. An output of the block 1404 is provided to an input of a PAR (spread) coding block 1405. An output of the block 1405 is provided to an input of a basis function generator 1406. An output of the basis function generator 1406 is provided to a first input of an adder **1419** ~~1491~~.

Please replace Page 32 second paragraph with the following rewritten paragraph:

Data for an *M*-th channel (i.e., channel *M*-1) of the *M*-channel band (i.e., Band 0) is provided to an input of an FEC block 1412. An output of the FEC block 1412 is provided to an input of an interleaver/scrambler block 1413. An output of the block 1413 is provided to an input of a modulator/mapper block 1414. An output of the block 1414 is provided to an input of a PAR coding block 1415. An output

of the block 1415 is provided to an input of a basis function generator 1416. An output of the basis function generator 1416 is provided to an M-th input of the adder **1419** ~~1491~~.

Please replace Page 32 third paragraph with the following rewritten paragraph:

An output of the adder 1419 is provided to an input of a windowing filter 1420. An output of the windowing filter **1420** ~~1421~~ is provided to an input of a sub-band filter 1421. An output of the sub-band filter is provided to a first input of an adder 1430. The transmitter structure for bands other than Band 0 is similar to that of Band 0. The adder 1430 has M_B ~~M_B-1~~ inputs, where M_B-1 ~~M_B~~ is the number of bands. Thus, the output of the adder 1430 is the sum of all bands 0 through M_B-1. The output of the adder 1430 is provided to a digital-to-analog converter (not shown) to convert the transmitter signal into an analog signal for transmission on the communication medium.

Please replace Page 36 first paragraph with the following rewritten paragraph:

An optional channel manager 1530 provides improved performance for the receiver 1500. A magnitude output and a phase output from each of the equalizers **1515** ~~1514~~ and **1525** ~~1524~~ are provided to respective inputs of the channel manager 1530. A clock control output from the channel manager 1530 is provided to a control input of the clock 1505. An AGC-control output from the channel manager 1530 is provided to a gain-control input of the AGC 1502.

Please replace Page 36 second paragraph with the following rewritten paragraph:

In the receiver 1500, the sub-band filter 1501 selects portions of the spectrum that correspond to the desired band. The sub-band filter 1501 can be implemented as an active filter, a passive filter, a Surface Acoustic Wave (SAW) filter, etc. The AGC 1502 adjusts the gain of the analog signal to a desired level. The spreading

decoder **1512 and 1522** ~~1504~~ decodes the spreading codes (if any) applied in the transmitter. The optional window blocks 1510 and 1520 provide pre-transform filtering of the spectrum for each of the desired channels within the band. The sliding-window transform blocks 1511 and 1521, the synchronization blocks 1514 and 1524 and the data aligner blocks 1513 and 1523 function as described previously herein (and as described, for example, in connection with Figures 10-13 and in copending U.S. Application No. 09/794761 hereby included by reference in its entirety). The equalizers 1515 and 1525 equalize the amplitude and phase of each channel. The demappers 1516 and 1526 map symbols back into data bits.

Please replace page 40 first paragraph with the following rewritten paragraph:

Figure 17B is a block diagram of a CORDIC processing element 1710 that implements the Type-2 transform shown in Figure 10B. In the processing element 1710, the input b_1 is provided to an input of a register 1701, and the input b_2 is provided to an input of a register 1702. An output of the register 1701 is provided to a first data input, x_k, of the rotation block 1703 and to the output b_1'. An output of the register **1701** ~~1702~~ is provided to a second input, y_k, of the rotation block 1703 and to the output b_2'. The input θ_k is provided to a rotation input of a CORDIC rotation block 1703. The rotation block 1703 provides the first data output, x_k', and the second data output, y_k'.

Please replace Page 42 first paragraph with the following rewritten paragraph:

In Figure 22, data from the analog-to-digital converter 323 is provided to an input of a z^{-N} time delay 2201 and to a first input of an adder 2202. An output from the time delay 2201 is provided to provided to an input of the z^{-N} time delay 2101 and to the second input of the adder 2102 (with a weight of **-2** ~~-3~~). An output of the time delay 2101 is provided to the input of the z^{-N} time delay 2102 and to the second input of the adder 2103 (with a weight of **1** ~~3~~). The output of the adder

2103 is provided to the first input of an adder 2104. The output of the time delay 2102 is provided to the second input of the adder 2104 (with a weight of –1). An output of the adder 2104 is provided to a first input of a multiplier 2105. A complex coefficient $e^{-j\omega_t n}$ is provided to a second input of the multiplier 2105. An output of the multiplier 2105 is provided to a first input of an adder 2106. An output of the adder 2106 is provided to an input of a z^{-1} time delay 2107 and to a first input of an adder 2108. An output of the time delay 2107 is provided to a second input of the adder 2106. An output of the adder 2108 is provided to an input of a z^{-1} time delay 2109 and to a first input of an adder 2203. An output of the adder 2203 is provided to an input of a z^{-1} time delay 2204 and as an output of the filtered Type-2 sliding window DFT. An output of the time delay 2204 is provided to a second input of the adder 2203

Please replace Page 42 second paragraph with the following rewritten paragraph:

Advantageously, the delay elements 2101, **2102** ~~2202~~, and 2201 operate on real numbers. The delay elements 2101, **2102** ~~2202~~, and 2201 can be shared between multiple bins or sub-carriers like the delay 1010 shown in Figures 10A and 10B. For each additional rectangular type filter of length N, the symbol length must be increased by N. In some systems this is acceptable. Even in systems where increasing the symbol length is unacceptable, the structure shown in Figures 21 and 22 can be used if it is desired that filtering be done on certain portions of the received signal, with no filtering (or other filtering) being done on the rest. An example could be for synchronization in the received signal. After the synchronization, the standard Type-2 sliding-window DFT (without additional rectangular filters) can be used for the remainder of the packet. This is useful when synchronization employs longer symbols than the data sections of the packet. Since the structures with integrated filters are similar, it is possible for a system to utilize the same structural components when this switch is made.